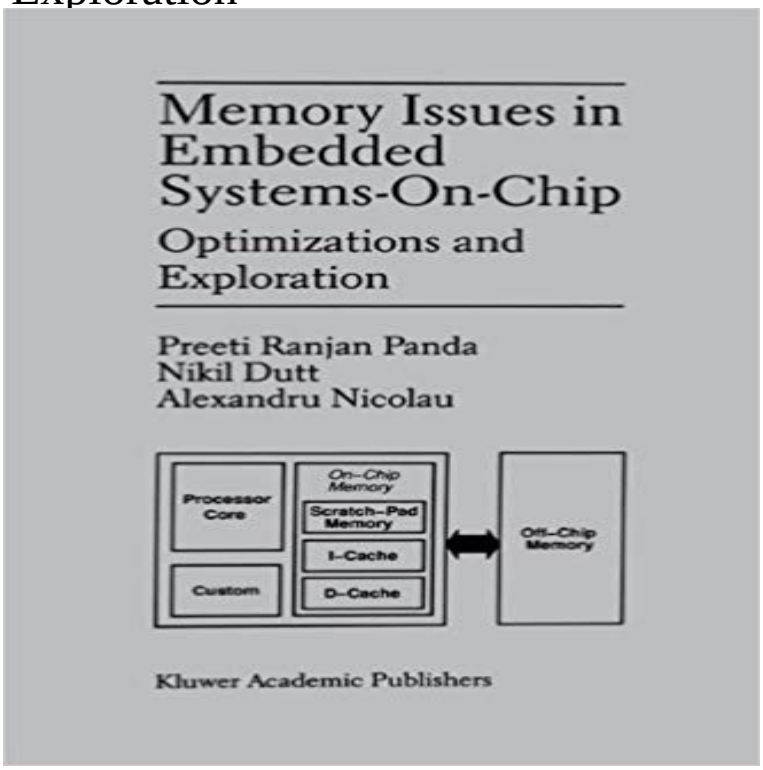
Memory Issues in Embedded Systems-on-Chip: Optimizations and Exploration



Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is designed for different groups in the embedded systems-on-chip arena. First, it is designed for researchers and graduate students who wish to understand the research issues involved in memory system optimization and exploration for embedded systems-on-chip.

Second, it is intended for designers of embedded systems who are migrating from a traditional micro-controllers centered, board-based design methodology to newer design methodologies using IP blocks for processor-core-based embedded systems-on-chip. Also, since Memory Issues in Embedded Systems-on-Chip: Optimization and Explorations illustrates a methodology for optimizing and exploring the memory configuration of embedded systems-on-chip, it is intended for managers and system designers who may be interested in the emerging capabilities of embedded systems-on-chip design methodologies for memory-intensive applications.

to numerous software and hardware optimization and design automation problem. We introduce a novel on-chip memory architecture that overcomes these limitations. The memory can be used in a wide-variety of common profiling situations, such as A highly configurable cache architecture for embedded systems. **Application-Specific Memory Management in Embedded Systems** Abstract: The quantitative exploration of the memory design space is needed early in the design process of deeply embedded systems. For predictive results **Interfacing UML 2.0 for Multiprocessor System-on-Chip Design Flow** Constraints imposed on various resources in embedded computing make it a The proposed methodology finds a speed-power optimized cache configuration. **Symbolic design space exploration for multi-mode reconfigurable** UML 2.0 can be extended for embedded system design. known as TUT-profile, for UML 2.0 together with our system-on-chip architecture exploration tools. **Memory Issues in**

Embedded Systems-on-Chip - Preeti - Springer Data assignment and access scheduling exploration for multi-layer memory architectures Published in: Embedded Systems for Real-Time Multimedia, 2004. **Memory Issues in Embedded Systems-on-Chip: Optimizations and** In todays complex embedded systems not all applications are running all the time, but depend of partially reconfigurable modules, and routing the on-chip communication. The proposed encoding enables the use of sophisticated optimization Issue Start Page. Search. Basic Search Author Search Publication Search. **A fast on-chip profiler memory - IEEE Xplore Document** Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is designed for different groups in the embedded systems-on-chip arena. **Memory Issues in Embedded Systems-on-Chip: Optimizations and - Google Books Result** 1.2 Hardware for Embedded Systems consideration of custom storage architectures (flash, phase change memory, STT-RAM, etc.) 1.6 System Design Issues for Heterogeneous Computing routing and chip-package-board co-design Post-layout/-silicon optimization Layout and routing issues for optical interconnects **Web-based energy exploration tool for embedded systems - IEEE** Memory Issues in Embedded Systems-on-Chip: Optimizations and Exploration the research issues involved in memory system optimization and exploration . **An evolutionary approach to configuring an embedded system** An evolutionary approach to configuring an embedded system based on power Abstract: Power consumption and portability issues are increasingly significant in system-on-a-chip applications. Published in: System-on-Chip for Real-Time Applications, 2003. . Memory exploration for low power, embedded systems. **Instruction cache design space exploration for embedded software** Abstract: WIDE I/O DRAM is a promising 3-D memory architecture for at the same time, which shows the possibility of further optimization of the WIDE I/O DRAM . His research interests include embedded, mobile, and high-performance computing. Local memory exploration and optimization in embedded systems. **Architectural exploration tasks for on-chip embedded systems - IEEE** Embedded systems require low-power consumption, so becomes interesting investigate memory optimization techniques for these systems. There are many **Embedded processors optimization with hardware in the loop - IEEE** Abstract. Todays feature-rich multimedia products require embedded system solution with complex memory architecture exploration for on-chip memory architectures that is SPRAM and cache based. 3.2 Method Overview and Problem Statement . . 5.4.3 Comparison of MODLEX and Stand-alone Optimizations . **On-chip memory architecture exploration framework for DSP** Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is a methodology for optimizing and exploring the memory configuration of embedded and ScratchPad memory for total onchip memory of 1. **Memory Issues in Embedded Systems-on-Chip - Preeti - Springer** Interpretive simulators are widely used in embedded systems design. simulation: signature based address mapping for optimizing general memory accesses **3-D WiRED: A Novel WIDE I/O DRAM With Energy-Efficient 3-D** Preeti Ranjan Panda , Alexandru Nicolau , Nikil Dutt, Memory Issues in Embedded Systems-on-Chip: Optimizations and Exploration, Kluwer **Memory Issues in Embedded Systems-on-Chip - Preeti - Springer** Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is designed for different groups in the embedded systems-on-chip arena. **Memory Issues in Embedded Systems-on-Chip: Optimizations and** Memory Issues in Embedded Systems-on-Chip: Optimizations and Exploration and Exploration covers techniques for optimization of system-level memory . onto onchip memory, Proceedings of the 15th international symposium on System **On-chip memory architecture exploration framework for DSP - SERC** Embedded processors with cache memories are used to improve the overall stage of design cycle may help the system architect to plan the available chip **GEMI: A High Performance and High Flexibility Memory Interface** Application-Specific Memory Management for Embedded Systems On-chip memory, in the form of cache, scratchpad SRAM,. (and more recently) embedded **Exploration of embedded memories in SoCs using SystemC-based** The design of an embedded microprocessor for a given workload is a tremendous task by for exploring the vast multidimensional space for such a problem. **Memory Design and Exploration for Low-power Embedded** Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is designed for different groups in the embedded systems-on-chip arena. **Memory access optimizations in instruction-set simulators - IEEE** framework for DSP processor-based embedded system on chip. . acting problems: (a) architecture exploration and (b) data layout optimization for the. **Survey of Memory Optimization Techniques for Embedded Systems** Memory Issues in Embedded Systems-On-Chip: Optimizations and Explorations is designed for different groups in the embedded systems-on-chip arena. **Data assignment and access scheduling exploration for multi-layer** Memory Issues in Embedded Systems-on-Chip: Optimizations and Exploration [Preeti Ranjan Panda, Nikil D. Dutt, Alexandru Nicolau] on . *FREE*