

Compilation Techniques for Reconfigurable Architectures



The extreme flexibility of reconfigurable architectures and their performance potential have made them a vehicle of choice in a wide range of computing domains, from rapid circuit prototyping to high-performance computing. The increasing availability of transistors on a die has allowed the emergence of reconfigurable architectures with a large number of computing resources and interconnection topologies. To exploit the potential of these reconfigurable architectures, programmers are forced to map their applications, typically written in high-level imperative programming languages, such as C or MATLAB, to hardware-oriented languages such as VHDL or Verilog. In this process, they must assume the role of hardware designers and software programmers and navigate a maze of program transformations, mapping, and synthesis steps to produce efficient reconfigurable computing implementations. The richness and sophistication of any of these application mapping steps make the mapping of computations to these architectures an increasingly daunting process. It is thus widely believed that automatic compilation from high-level programming languages is the key to the success of reconfigurable computing. This book describes a wide range of code transformations and mapping techniques for programs described in high-level programming languages, most notably imperative languages, to reconfigurable architectures.

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